

FIG.1



The diagram illustrates a TFT array 10A. It features a 3x4 grid of pixels. Each pixel is driven by a TFT (Thin-Film Transistor) with gate (G), drain (D), and source (S) regions. The source of each TFT is connected to a common line (COM) and a load capacitor (CLC). The gate of each TFT is connected to a gate line (Lg). The drain of each TFT is connected to a data line (Ld). The array is driven by gate lines (Lg) and data lines (Ld).

FIG.3

**RESPONSE SPEED TO LIQUID CRYSTAL CELL GAP
(MEASURED VALUES)**

CELL GAP	RISING RESPONSE TIME	FALLING RESPONSE TIME
4.8 μm	5.85ms	26.03msec
1.5 μm	0.73ms	5.5msec

FIG.4

FIG.5A

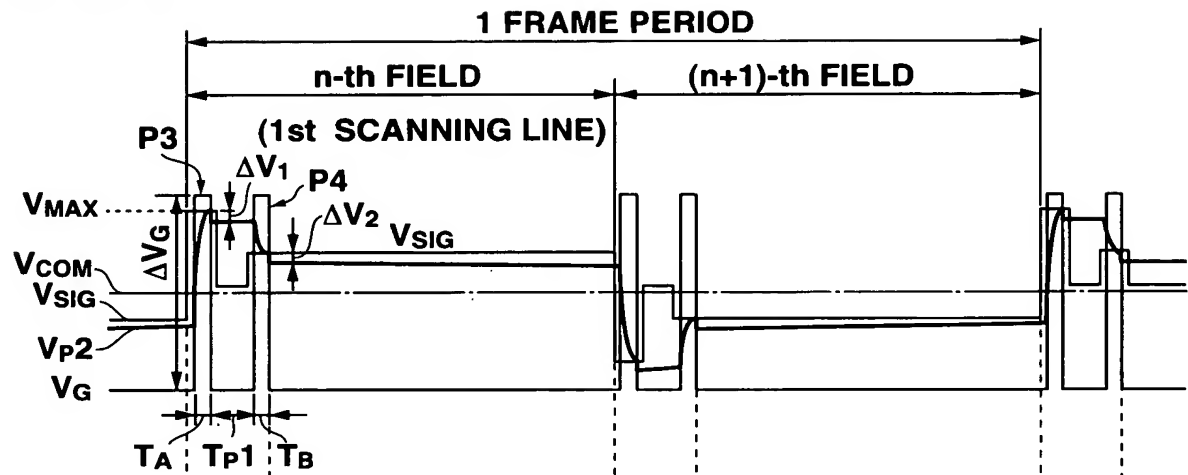


FIG.5B

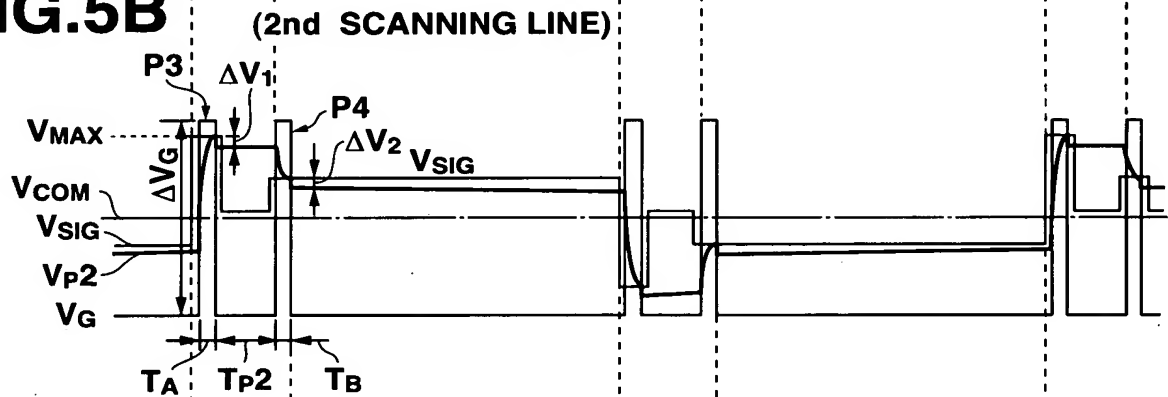
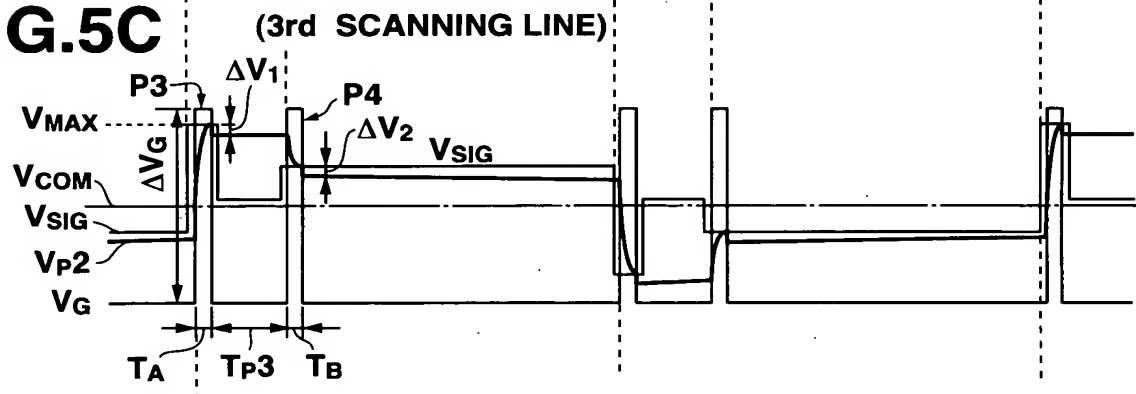


FIG.5C



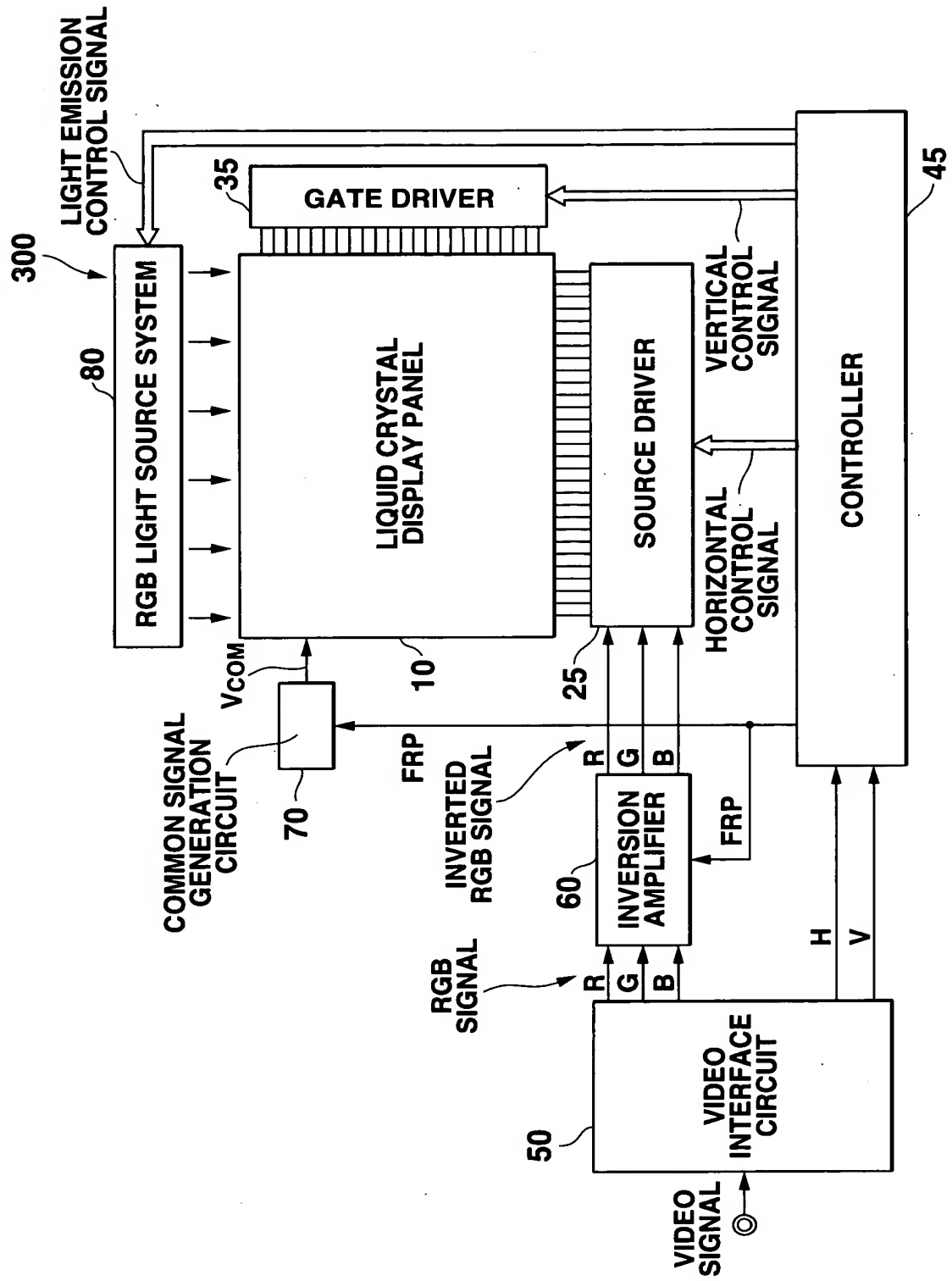


FIG. 6

FIG.7A

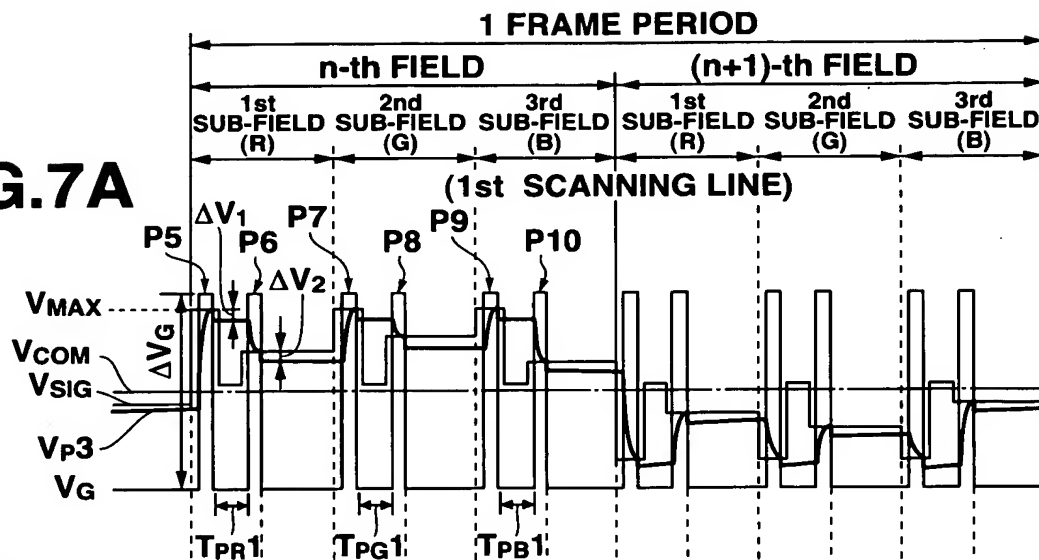


FIG.7B

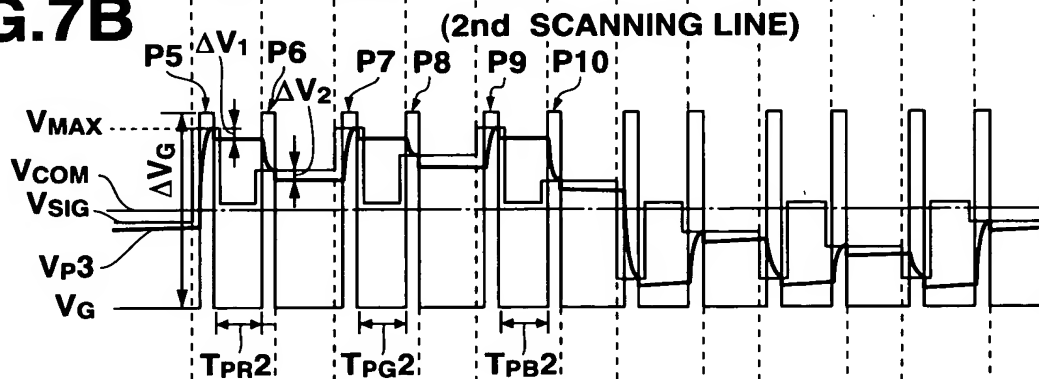


FIG.7C

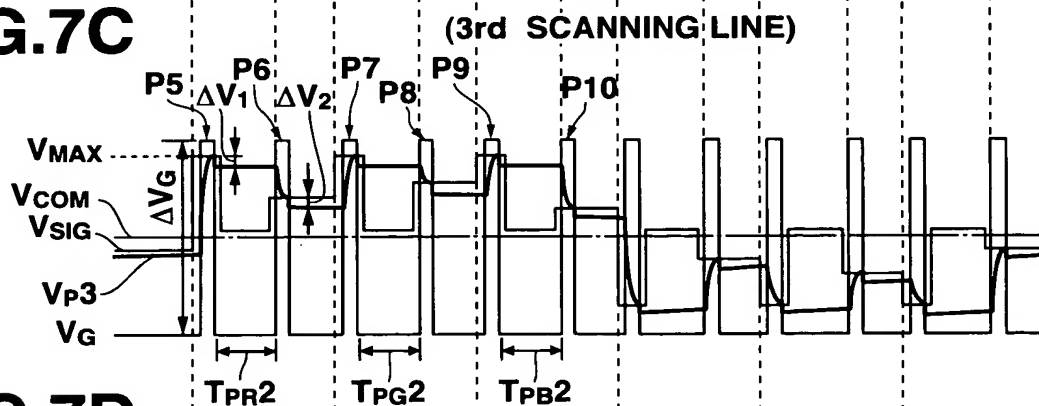
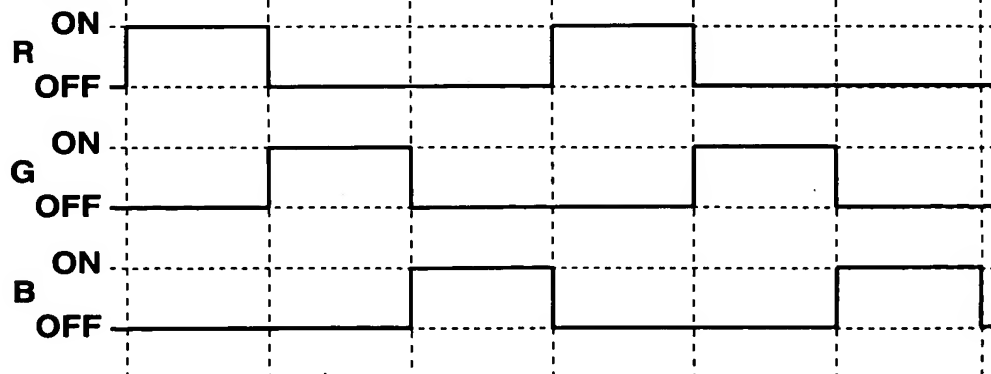


FIG.7D



400484-10204

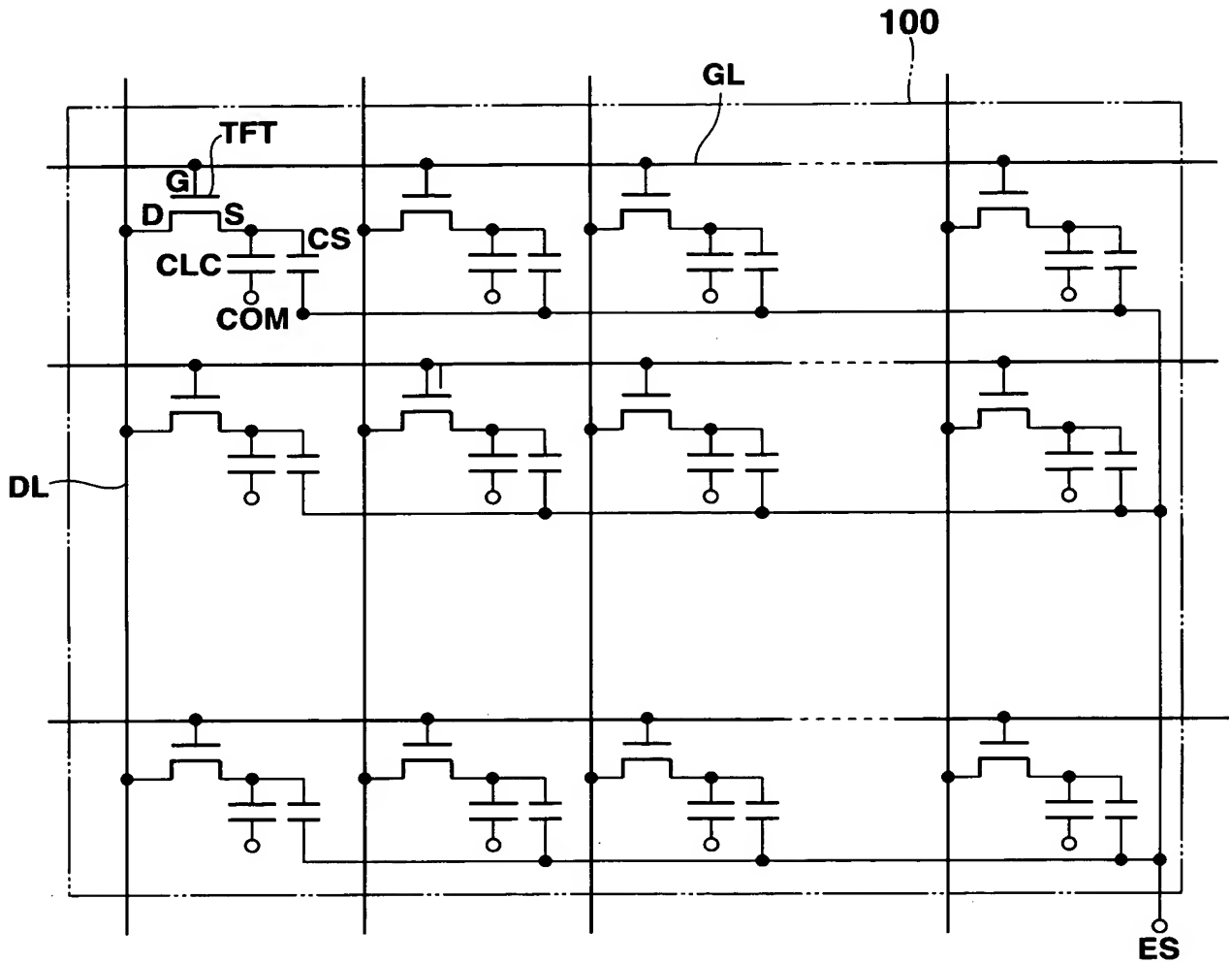


FIG.8A
PRIOR ART

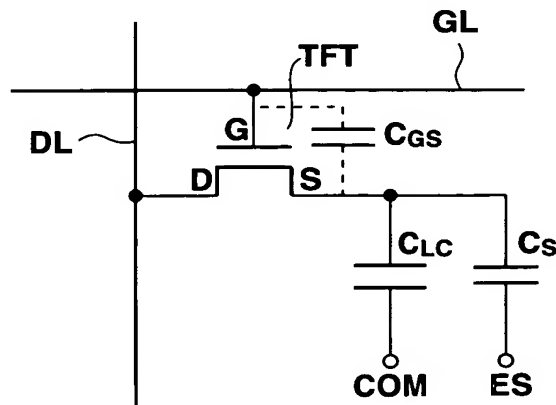


FIG.8B
PRIOR ART

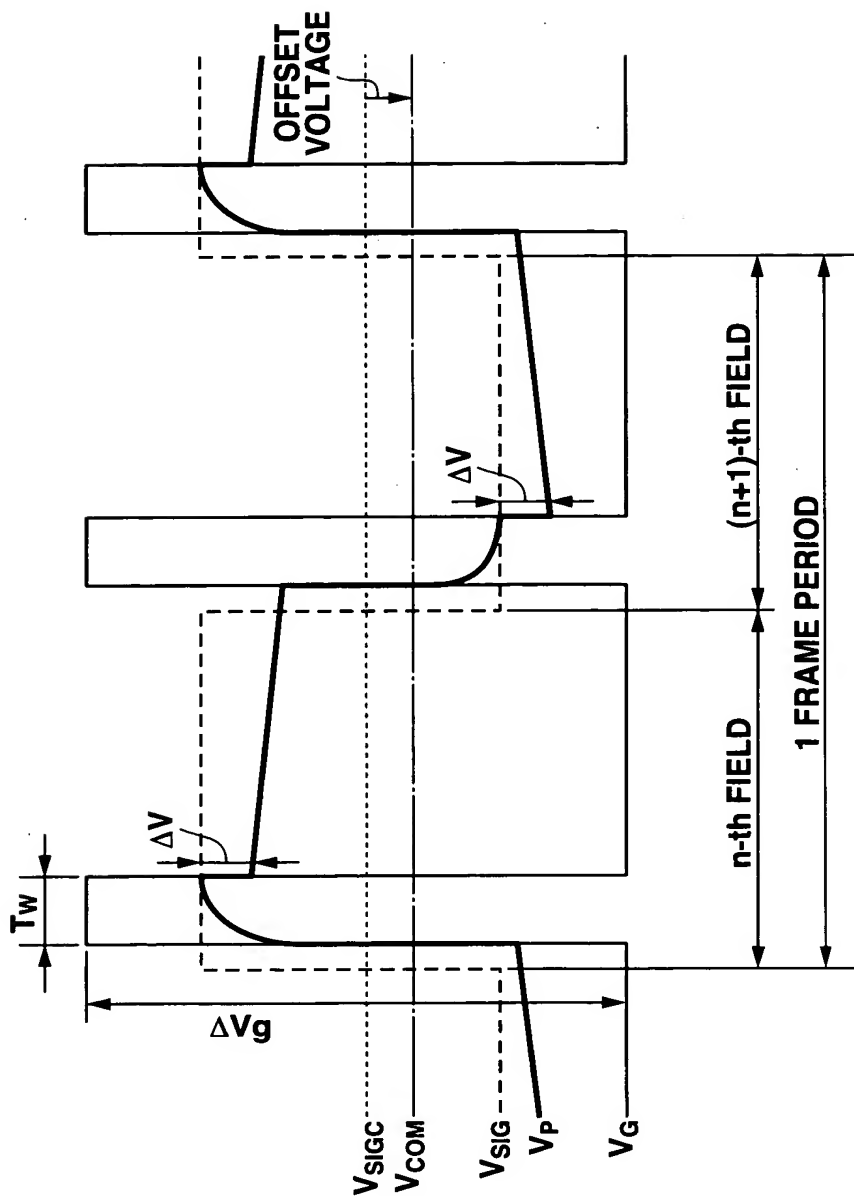


FIG.9
PRIOR ART

FIG. 10 - 8942000

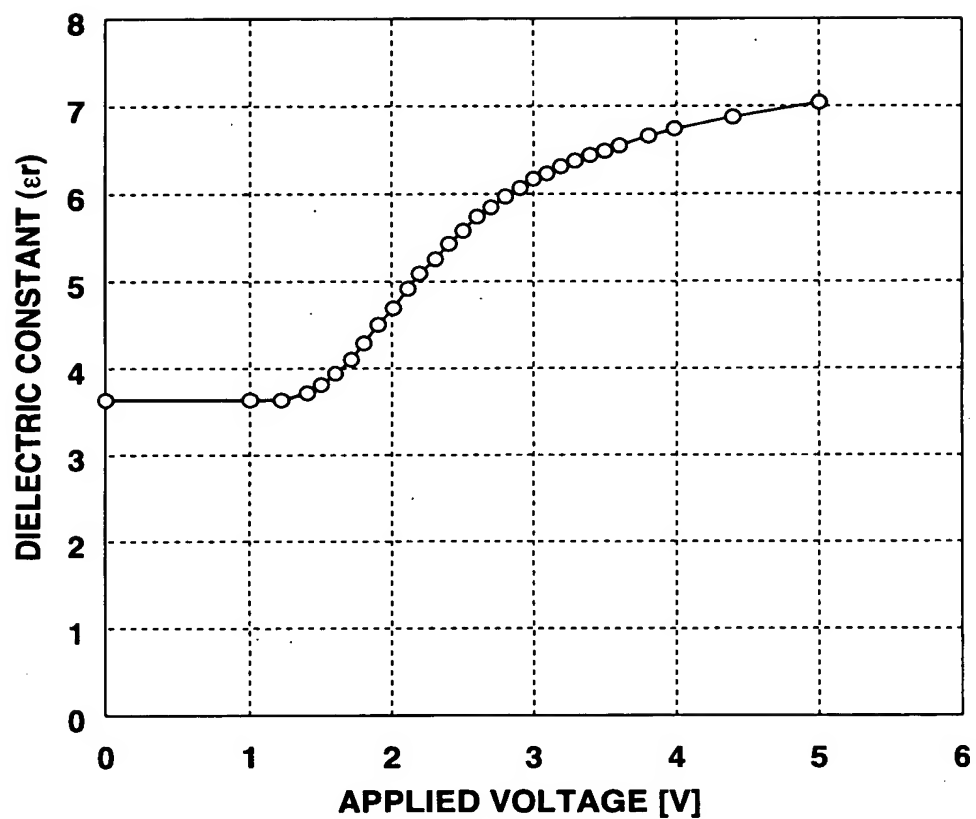


FIG.10
PRIOR ART